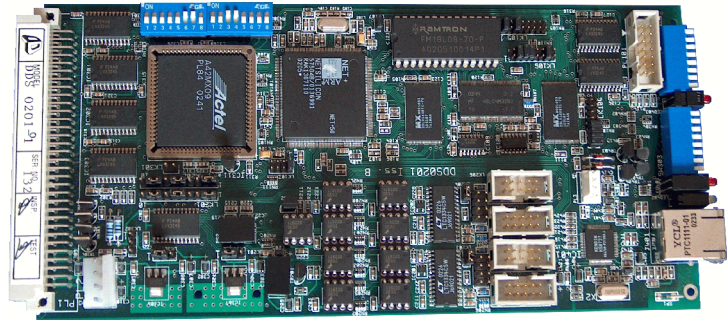


DOUBLE D ELECTRONICS LTD

DDS0201 ARM SLAVE PROCESSOR BOARD

- * 10/100Base T Network Interface
- * Two RS-232/422/485 Serial ports
- * Optoisolated Serial Ports
- * Option Switches
- * 4Mbyte Flash Program Memory
- * 16Mbyte SDRAM Data memory
- * Versatile Host Processor Interface
- * Status LEDs
- * Alarm relay interface
- * JTAG emulator connection



This board uses an ARM-based processor subsystem to support two main types of application:

- Standalone applications involving two serial ports and optionally a network interface.
- Applications where this board provides a communications slave processor. The host processor interface provides three access modes - FIFO, pseudo-FIFO and dual port RAM.

The heart of the board is the NetSilicon NET/ARM+50 processor, which provides all the key functions. Additional circuitry implements the optional host interface, which supports both the FIFO and the shared RAM modes of the ENI interface. From the host perspective the shared RAM may be accessed either directly as a memory block, or in an indirect manner using a data register and an autoincrementing pointer register.

Two electrically isolated serial ports provide RS-232/RS-422/RS-485 capability, including a full set of modem control signals on the RS-232 interface.

Two open collector outputs can be used to switch external circuitry; typically alarm or status relays.

A number of LED indicators at the front of the board show the status of the network link, and two indicators may be driven directly by the processor to signal software status.

Software development is facilitated by a connector for a JTAG emulator.

Ordering Information

DDS0201-01 Fully populated processor board, including network status LEDs, front panel, RS-422/485 optimised serial connectors.

DDS0201-02 Processor board excluding host interface; including network status LEDs, front panel, RS-422/485 optimised serial connectors.

DDS0201-03 Processor board excluding host and network interfaces; includes front panel, RS-422/485 optimised serial connectors.

For RS-232 optimised connectors, part number becomes DDS0201-1X

SPECIFICATION

- Physical:** Extended Single Eurocard, 100 x 220mm
Optional 8HP front panel to accept serial connectors
- Power:** 5V d.c. \pm 5%
DDS0201-X1 - 1000mA maximum
DDS0201-X2 - 800mA maximum
DDS0201-X3 - 700mA maximum
- Processor:** Net/Arm+50 processor with 100BaseT MAC and peripherals
4Mbyte flash memory (32-bit wide)
16Mbyte SDRAM (32-bit wide)
32Kbyte FRAM or EEPROM non-volatile memory (8-bit wide)
- Connectors:** RJ-45 network connection
10-way IDC plugs for serial - if used with standard ribbon cables give the following options:
a) PC-compatible RS-232 port on 9-D plug
b) SA-Bus compatible RS-422/485 port with transmit clock on 9-D socket.
DIN41612 Type C (64-way) for host interface
4-way 0.1" pitch Molex header for alarm/relay drives
14-way IDC for JTAG emulator
- Network:** 10/100 BaseT on standard RJ-45 connector. Status LEDs on board
- Serial:** Two full-featured serial ports implemented, each with individual electrical isolation using optoisolators and individual on-board d.c. to d.c. converters. Nominal 50V isolation.
- RS-232:** Full PC-compatible hardware functionality - includes modem control signals. Link options for transmit/receive clocks.
- RS-422/485:** Transmit data enabled by RTS or on-board link.
One further output signal, linkable as transmit clock, receive clock, DTR.
Receive data.
One further input signal, linkable as transmit clock, receive clock, CD, DSR.
Receive signals have link-enabled termination/biasing networks.
- DIP Switch:** Two 8-way DIP switches, accessible through panel; can be read by software.
- Host:** Host connector implements an 8-bit processor interface, with separate memory and I/O address spaces.
FIFO interface of ENI accessible via I/O registers.
Dual port RAM of ENI accessible either directly through the memory address space, or indirectly using a data register and autoincrementing pointer register in the I/O address space.
Various control functions available through the I/O address space, including processor reset.
- Support:** Modified version of NetSilicon BSP available